

A Speed-up Hardware Architecture for CCMP Encryption Protocol

Abstract of the Disclosure

5 A speed-up hardware architecture used in wireless encryption/decryption operation comprises: a plurality of operation units, that each operation unit is capable of accomplishing a designated operation independently, further comprising: a data receiving device having two inputs that a first input is used for receiving an external data signal and a second
10 input is used for receiving a supporting signal coming from the other operation unit, wherein when an operating mode of the data receiving device is “normal”, the data receiving device will output the first input, and when an operating mode of the data receiving device is “speed-up”, the data receiving device will output the second input; and an operating device
15 coupling to the data receiving device for processing the data from the data receiving device and outputting the processed data thereafter; and a control unit coupling to every operation unit in the architecture for enabling the operation units which are idle to assist the working operation units for data processing, further comprising: a controlling device coupling to the data
20 receiving device of every operation unit in the architecture for issuing a control signal and changing operating mode; and an integrating device coupling to the operating device of every operation unit in the architecture for integrating outputs coming from the operating devices of operation units which are in “speed-up mode”.

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